Memristors and Memristive Systems

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Four Basic Circuit Variables

- **Voltage**: \( v(t) \)
- **Current**: \( i(t) \)
- **Charge**: \( q(t) \triangleq \int_{-\infty}^{t} i(\tau) \, d\tau \), or \( i = \frac{dq(t)}{dt} \)
- **Flux**: \( \phi(t) \triangleq \int_{-\infty}^{t} v(\tau) \, d\tau \), or \( v = \frac{d\phi(t)}{dt} \)
Four Basic Circuit Variables

\[ i(t) \]

\[ v(t) \]

\[ q(t) \triangleq \int_{-\infty}^{t} i(\tau) d\tau \]

\[ \phi(t) \triangleq \int_{-\infty}^{t} v(\tau) d\tau \]

\[ \text{voltage} \quad \nu(t) \]

\[ \text{current} \quad i(t) \]

\[ \text{charge} \quad q(t) \]

\[ \text{flux} \quad \varphi(t) \]
### Three Basic Circuit Elements

#### Capacitor (1745)
- **Formula:** \( i(t) = C \frac{dv(t)}{dt} \)
- **Equation:**
  - Current: \( i(t) \)
  - Voltage: \( v(t) \)
  - Capacitance: \( C \)

#### Resistor (1827)
- **Formula:** \( v(t) = R \ i(t) \)
- **Equation:**
  - Voltage: \( v(t) \)
  - Current: \( i(t) \)
  - Resistance: \( R \)

#### Inductor (1831)
- **Formula:** \( v(t) = L \frac{di(t)}{dt} \)
- **Equation:**
  - Voltage: \( v(t) \)
  - Current: \( i(t) \)
  - Inductance: \( L \)
Resistor

Linear resistor: $v = Ri$ or $i = Gv$
**Capacitor & Inductor**

**Capacitor**

\[ q = C \cdot v \]

- **Linear Capacitor**
  - \( C = \text{Capacitance, in Farads (F)} \)

**Inductor**

\[ \varphi = L \cdot i \]

- **Linear Inductor**
  - \( L = \text{Inductance, in Henry (H)} \)
Three Passive Circuit Elements

$v, i, q, \phi$ are the 4 key variables in electrical systems

RLC elements are characterized by:

- $v = R \cdot i$ (Resistor)
- $q = C \cdot v$ (Capacitor)
- $\phi = L \cdot i$ (Inductor)
Four Passive Circuit Elements

\( v, i, q, \phi \) are the 4 key variables in electrical systems.

RC elements are characterized by:

\[ v = R \cdot i \quad \text{(Resistor)} \]
\[ q = C \cdot v \quad \text{(Capacitor)} \]
\[ \phi = L \cdot i \quad \text{(Inductor)} \]

Missing relationship between \( \phi \) and \( q \):

\[ \phi = f(q) \]
\[ v = M(q) \cdot i \quad \text{(Memristor)} \]
4th Circuit Element: Memristor

• Charge-flux relationship
  – Memristor uniquely defines the constitutive relation of $\varphi = f(q)$.
  – Memristance can be found as $df(q)/dq$, in its valid memristive operation.

\[ \varphi = f(q) \quad \text{time derivatives} \quad \frac{d\varphi}{dt} = \left\{ \frac{d}{dq} f(q) \right\} \cdot \frac{dq}{dt} \]

Constitutive relationship between charge ($q$) and flux-linkage ($\varphi$)

• Memristor (Memory resistor)
  – Resistively connects voltage and current: $v = M(q) \cdot i$
  – Its resistance is a function of $q$ (current integration)
Circuit Element: Memristor

- Passive two-terminal device
- Exhibits static flux-charge relationship
- A resistor that changes (programs) its resistance with the entire history of input
- In other words, it is a device that retains a memory of its prior states
History of Memristor

- 2008, “The missing memristor found”, Nature
Memristive Systems (1976)

- Defined by L. Chua & S.M. Kang
  - A class of nonlinear devices whose dynamics is controlled by state variables that incorporate memory effects
    \[
    \begin{align*}
    v &= M(\bar{x}, i) \cdot i \\
    d\bar{x} &= dt \cdot f(\bar{x}, i) \\
    i &= W(\bar{y}, v) \cdot v \\
    d\bar{y} &= dt \cdot g(\bar{y}, v)
    \end{align*}
    \]

- Examples
  - Hodgkin-Huxley equation, fluorescent lamp, thermistor, etc.
  - Memristor is a special case of memristive systems
    \[
    \begin{align*}
    v &= M(q) \cdot i \\
    dq &= dt \cdot i \\
    i &= W(\varphi) \cdot v \\
    d\varphi &= dt \cdot v
    \end{align*}
    \]

Current-controlled memristor

Voltage-controlled memductor

As the 4th Basic Element

Memristor
was postulated in 1971

Leon O. Chua
Memristor: The missing circuit element

and found in 2008

D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams
The Missing Memristor Found
HP TiO$_2$ Memristor (2008)

\[ v = M(q) \cdot i \]

Memristance

\[ M(q) \triangleq R_{OFF} \left( 1 - \frac{\mu_v R_{ON}}{D^2} \frac{q}{i} \right) \]
HP TiO$_2$ Memristor (2008)

AFM image of memristor crossbar at 17nm

The smallest virus:
~25 nm in dia

Fabricated by
Imprint Lithography –
Can be stacked for
Higher area density

(cell density : 100 Gbit/cm$^2$)
8nm Memristor by UMASS (2013)

From:
S. Pi, P. Lin, Q. Xia, “Cross point arrays of 8 nm × 8 nm memristive devices fabricated with nano imprint lithography”, J. Vac. Sci. Technol. B 31, 06FA02-1 - 06FA02-6, 2013
Multi-stacked Memristors Concept by HP

The entire *library of congress* can be stored in a multi-layer Hp memristor chip

library of Congress

21,218,408 books
10 terabytes \((10^{12})\)
Transistors vs. Memristors

As nano devices shrink below 20 nm, *transistors* begins to fail, while the *memristor* phenomenon begins to dominate, and the circuit dynamics becomes increasingly nonlinear.
Footprint of Memristors

- **Distinctive features**
  - Resistance of the device is determined by the entire history of input
  - Frequency dependent dynamics (linear resistor at high freq)
  - Manipulates “Pinched Hysteretic Loops” in voltage-current dynamics

**Memristor as 4\textsuperscript{th} fundamental device**
Prof. Chua’s Experimental Definition of the Memristor

If it’s Pinched
It’s a Memristor

Diagram showing the relationship between voltage (v) and current (i).
Memristor Materials

- Many combinations….
  - Ti/TiO2/Ti
  - Ti/TiO2/Pt
  - Al/TiO2/Al
  - Pt/TiO2/Pt
  - Pt/TaO5/Pt
  - TiN/WO3/TiN
  - TiN/Ti/HfO2/TiN
  - TiN/ZnO/Pt
  - Pr/ZrO2/Pt
  - Pt/NiO/Pt
  - Ag/TiO2/Au
  - ….
ECM, VCM, PCM

ECM
Active electrode

VCM
Inactive electrode

PCM
Inactive electrode

Solid electrolyte

TE

BE

Inactive electrode

Off state

On state
Basics and Phenomenology

- Metal-Insulator-Metal Structure
  insulator = ion conducting or mixed ionic-electronic oxides, chalcogenides, ionic solids

- Controlled breakdown
- Based on internal redox reactions - electrochemical and thermochemical effects
- First observation in 1960th but forgotten because of Si-based memories (EEPROM and DRAM)
- Many different names – RRAM, ReRAM, memristor or memristive devices, electroresistive memories, CBRAM
- Pinched hysteresis I-V loop

Current and resistance response to triangular or sinusoidal voltage sweep for bipolar cell
Basics and Phenomenology

- Often require initial electroforming step
- RESET = setting the device to high resistive state (also called erase or programming to the OFF state)
  - SET is the opposite
- Above certain threshold voltage Vset and Vreset the cell changes resistance rapidly
- Dotted line = current compliance
- Intermediate states (multilevel switching) by different current compliance
- The state can be read with relatively small Vread

Current and resistance response to triangular or sinusoidal voltage sweep for bipolar cell
Forming Process

- Very often need electroforming step
- Electroforming produce filament
- Single crystal require 10 – 100 V and long time (hours to break), thin films of the order of few volts and seconds
- Forming voltage is proportional to film thickness of I layer (field dependence) which is not the same for subsequent switching
- Electrical breakdown $\rightarrow$ local Joule heating in localized channel $\rightarrow$ Morphological and redox changes
- Current compliance to control the size of the channel

![diagram showing forming process with states: insulating, forming, gap, intermediate, metallic, virgin, off, on, and a graph showing voltage and current]
Technology & Devices

Most important issues:

• Reliability (device to device and cycle to cycle variance)

• Endurance (limited number of times the cell can be switched)

• Retention
Reliability

- Problems due to
  - Random walk of ions
  - Irregular atomic structure

Yield and ...

Weibull distribution of Ron and Roff values in 1 kbit 1T1R Ru/Ta2O5/TiO2/Ru VCM cells

...threshold variations in Ag/p-Si/Pt ECM
Endurance

- How many write cycles can be performed before it falls out of predefined acceptance window

- Limited endurance due to
  - Morphological changes
    - Gradual growth or dissolution of phases
  - Oxydation and/or drift of electrode material
  - Leakage of oxygen
Retention

• One or all states are thermodynamically metastable
→ High activation energy for hopping but with possible tradeoff to endurance
• Accelerated life time test by heating and extrapolation with Arrhenius plot
RRAM FPGA Integration

FPGA Chip

Cross-section View

Programmable Resistor

RRRAM – 3D Integration

10^{12} cycles

\[ \begin{align*}
\text{Current (A)} & \\
\text{\# of cycle} & \\
\end{align*} \]

Pt/TaOx/Ta_2O_5/Pt

V_{\text{set}} = 4.5 V, V_{\text{reset}} = 7.0 V, t_{\text{w}} = 10 \text{ ns}

– LRS – HRS

VLSI’11 (Samsung)
VLSI’12 (Samsung)

Multi-bit

Cumulative probability (%)

Log (I)

VLSI’11 (Stanford)

Bit-Cost Scalable

I_{\text{PROG}} < 100 \text{ nA}

Reset

Set

23 nA

50 nA

Current (A)

Voltage (V)

VLSI’11 (Stanford)

IEDM’12 (Stanford)

40 nm

VRRAM

Metal

SiO_2

Metal

SiO_2

Metal

SiO_2

Metal

HfO_x

Pt

SiO_2
3D RRAM

M.-C. Hsieh et al., IEDM 2013 (TSMC)

S. Yu, H.-Y. Chen et al., Symp. VLSI Tech. 2013
Bringing Memristive Memories to Market

- Adesto Technology: **Conductive Bridge RAM (CBRAM)**
Memristors as Nonvolatile Memories

Non-Volatile Nano Memristors will eventually replace the following conventional computer memories:

• Flash Memories
• DRAMs
• Hard Drives
Learning: Habituation

Déjà vu response is learning to recognize and ignore benign and boring stimulus.

**Excitation**

![Graph showing excitation](image)

**Response**

![Graph showing response](image)
Habituation in a Memristor

(a) Sensory Neuron
Stimulus

(b) Circuit diagram

(c) Graphs of $i(t)$ in Amps and $v(t)$ in Volts over time in seconds
Associative Learning

<table>
<thead>
<tr>
<th>Stimulus</th>
<th>Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unconditioned stimulus (UCS)</td>
<td>Unconditioned response (UCR)</td>
</tr>
<tr>
<td>Conditioned response (CS)</td>
<td>Conditioned response (CR)</td>
</tr>
</tbody>
</table>

**Pavlov’s Nobel-Prize Winning Experiment**

1. Before Conditioning
   - Food (Unconditioned Stimulus) → Salivation (Unconditioned Response)

2. Before Conditioning
   - Bell (Neutral Stimulus) → Salivation (No Conditioned Response)

3. During Conditioning
   - Bell (Neutral Stimulus) + Food (Unconditioned Stimulus) → Salivation (Conditioned Response)

4. After Conditioning
   - Bell (Conditioned Stimulus) → Salivation (Conditioned Response)

*Ivan P. Pavlov*
Memristor Circuit for Emulating Pavlov’s Dog

Associative Learning with Temporal Contiguity in a Memristive Circuit for Large-Scale Neuromorphic Networks
Memristor Circuit for Emulating Pavlov’s Dog
Amoeba Experiment

Digitally controlled video camera recording and processing system

Temperature-controlled Air Pump

Temperature-controlled chamber

amoeba crawling to the right

Graph showing temperature over time:
- Temperature range: 23°C to 26°C
- Time: 0 to 5 hours

Graph of temperature over time:
- Temperature at t=0 is 23°C
- Temperature at t=1 to t=2 is 26°C
- Temperature at t=2 to t=3 is 23°C
- Temperature at t=3 to t=4 is 26°C
- Temperature at t=4 to t=5 is 23°C
Amoeba Experiment

Temperature (°C)

Speed (mm/10 min)

Amoeba stops moving
Memristor Circuit Emulating Amoeba Exp.
Memristor Circuit Emulating Amoeba Exp.
1961 Nobel Prize in Physiology

Sir A. L. Hodgkin

Sir A. F. Huxley

Hodgkin-Huxley Nerve Membrane Model

From A.L. Hodgkin and A. F. Huxley
A Quantitative Description of Membrane Current and its Application to Conduction and Excitation in Nerve.

Memristance as Synaptic Weight

Tuning the *synaptic weight* during *learning* is equivalent to *biasing* the operating point with the corresponding *slope*.
Memristors as Artificial Synapses

- Memristors directly implement the synaptic plasticity

\[ v = M(q) \, i \]

\( M(q) \) is continuously tunable between \( R_{ON} \) and \( R_{OFF} \)

No need for space consuming complicated CMOS circuits

CMOS synapse emulating a learning rule called:
Spike Timing Dependent Plasticity (STDP)

1 memristor directly implements STDP

\[ < 30 \times 30 \, \text{nm}^2 \]

- Jo et al., Nanoletters 2010
Memristor STDP: Experimental Implementation

Jo et al., Nanoletters 2010

Memristor STDP curve

Bi & Poo 1998
Memristors as Artificial Synapses

- Memristors are small (< 50 x 50 nm²)

interconnection issue: about $10^4$ synapses per neuron in the brain

ex: CMOS “neurons” + memristive “synapses”

memristor crossbar arrays

No demonstration yet of operational mixed memristor/CMOS cognitive chip

to be solved: cross-talk, sneak paths, lithography
Computing: Von Neumann vs. Neuromorphic

- **Human brain**

<table>
<thead>
<tr>
<th>parallel architecture</th>
<th>analog</th>
</tr>
</thead>
<tbody>
<tr>
<td>$10^{11}$ neurons</td>
<td>10 Hz</td>
</tr>
<tr>
<td>$10^{15}$ synapses</td>
<td>20 W</td>
</tr>
</tbody>
</table>

- **Simulations of mouse cortex on Blue Gene L**

<table>
<thead>
<tr>
<th>Von-Neumann architecture</th>
<th>digital</th>
</tr>
</thead>
<tbody>
<tr>
<td>$8 \times 10^4$ neurons</td>
<td>1 GHz</td>
</tr>
<tr>
<td>$5 \times 10^{10}$ synapses</td>
<td>40 kW</td>
</tr>
</tbody>
</table>

*super-computers slower than mouse ($\times 10$)*
Computing: Biological Synapse vs. Memristor

**Synapses**

\[ 10^{10} / \text{cm}^2 \text{ (human cortex)} \]

\[ \frac{dw}{dx} = Ky(x - w) \]

**Nanoscale memristors:**

\[ 10^{11} / \text{cm}^2 \]

\[ \frac{dw}{dt} \equiv A(w_0 - w) + f(w) \sinh(Bv) \]
Summary & Conclusion

– Synapses are made of memristors
– Axons are made of memristors
– Brains are made of memristors

Memristors are the right stuff for making brainlike computers.