CD4073B, CD4081B, CD4082B Types

CMOS AND Gates

High-Voltage Types (20-Volt Rating)

CD4073B Triple 3-Input AND Gate
CD4081B Quad 2-Input AND Gate
CD4082B Dual 4-Input AND Gate

■ CD4073B, CD4081B and CD-4082B AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of CMOS gates.

The CD4073B, CD4081B, and CD4082B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

■ Medium-Speed Operation — t_{PLH}, t_{PHL} = 60 ns (typ.) at V_{DD} = 10 V
■ 100% tested for quiescent current at 20 V
■ Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
■ Noise margin (full package-temperature range) =
    1 V at V_{DD} = 5 V
    2 V at V_{DD} = 10 V
    2.5 V at V_{DD} = 15 V
■ Standardized, symmetrical output characteristics
■ 5-V, 10-V, and 15-V parametric ratings
■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
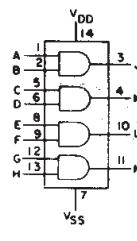
CD4081B FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  Voltages referenced to V_{SS} Terminal) .... –0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... –0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
  For T_A = –55°C to +100°C 500mW
  For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING–TEMPERATURE RANGE (T_A) .... –55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... –65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C

CD4082B FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, Input t_r,t_f=20 ns, and C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS
	V_{DD} Volts	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}	5	125	250	
	10	60	120	ns
	15	45	90	
Transition Time, t_{THL}, t_{TLH}	5	100	200	
	10	50	100	ns
	15	40	80	
Input Capacitance, C_{IN}	Any Input	–	5	7.5	pF
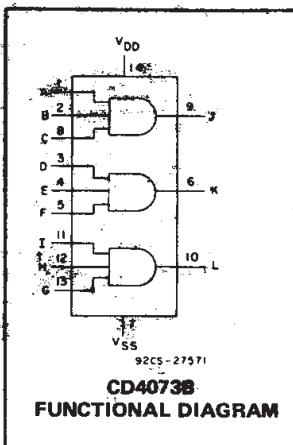
CD4073B FUNCTIONAL DIAGRAM

CD4073B, CD4081B, CD4082B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER-ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min. (+25)	Typ. (+25)	Max. (+25)	
Quiescent Device Current, I_{DD} Max.	—	0,5	5	0.25	0.25	7.5	7.5	—	0.01	0.25	µA
	—	0,10	10	0.5	0.5	15	15	—	0.01	0.5	
	—	0,15	15	1	1	30	30	—	0.01	1	
	—	0,20	20	5	5	150	150	—	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V_{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V_{IL} Max.	0.5	—	5	1.5				—	—	1.5	V
	1	—	10	3				—	—	3	
	1.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	V
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	—	±10⁻⁵	±0.1	µA
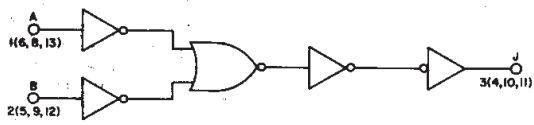
Fig. 3 — Typical voltage transfer characteristics.
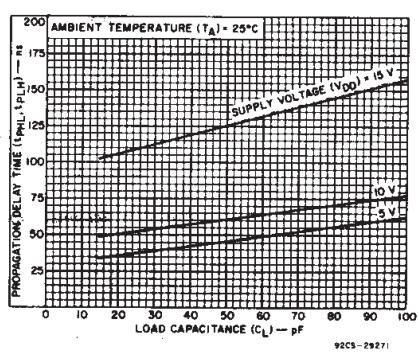
Fig. 4 — Typical propagation delay time as a function of load capacitance.
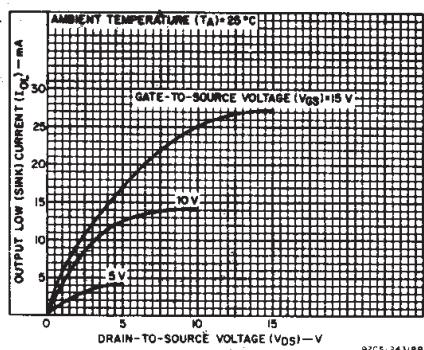
Fig. 5 — Typical output low (sink) current characteristics.
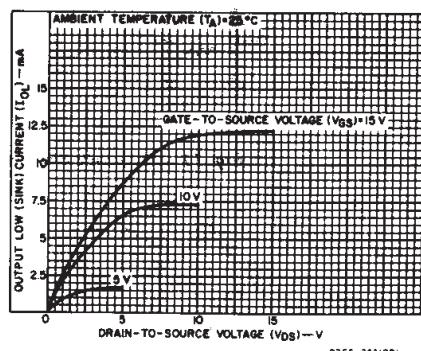
Fig. 6 — Minimum output low (sink) current characteristics.
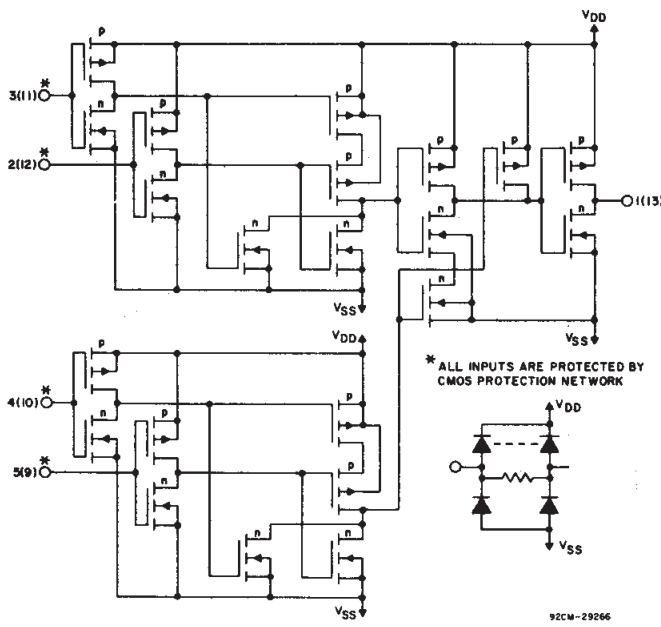

※ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

Fig. 1 — Schematic diagram for CD4081B (1 of 4 identical gates).

Fig. 2 — Logic diagram for CD4081B (1 of 4 identical gates).

Fig. 7 — Schematic diagram for CD4082B (1 of 2 identical gates).

*ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

Fig. 9 — Logic diagram for CD4082B (1 of 2 identical gates).

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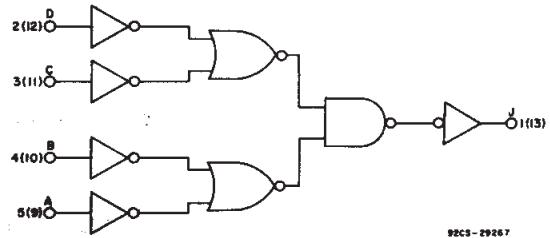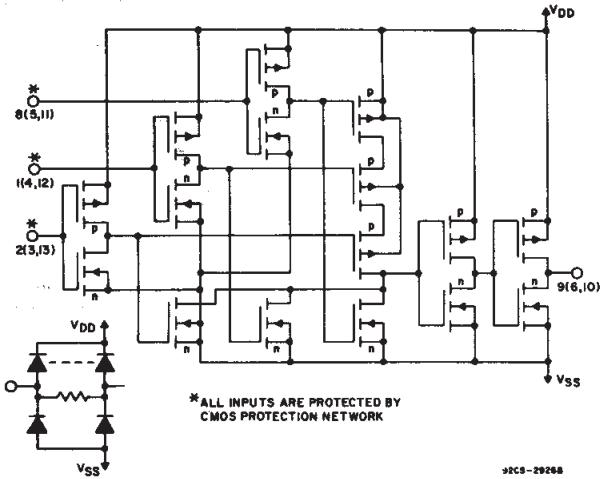
Fig. 11 — Schematic diagram for CD4073B (1 of 3 identical gates).
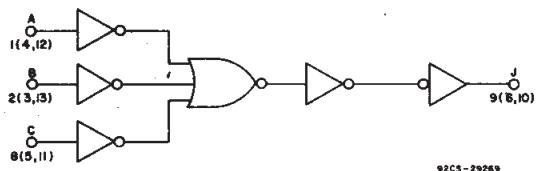
Fig. 13 — Logic diagram for CD4073B (1 of 3 identical gates).
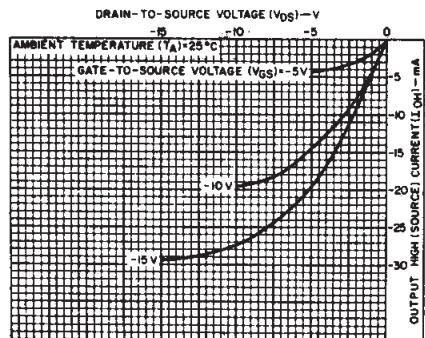
Fig. 8 — Typical output high (source) current characteristics.
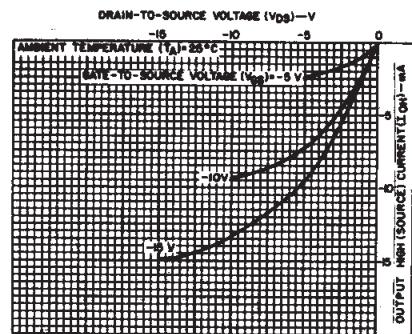

Fig. 10 — Minimum output high (source) current characteristics.
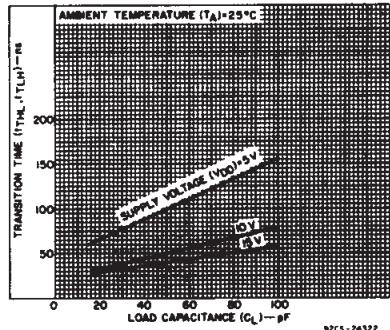
Fig. 12 — Typical transition time as a function of load capacitance.
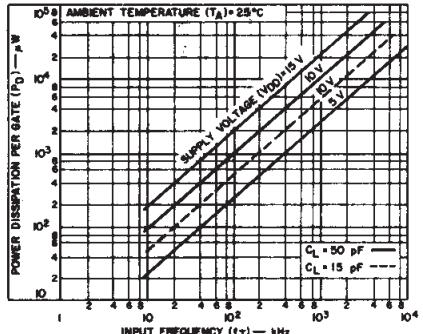
Fig. 14 — Typical dynamic power dissipation per gate as a function of frequency.
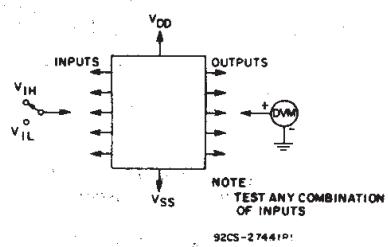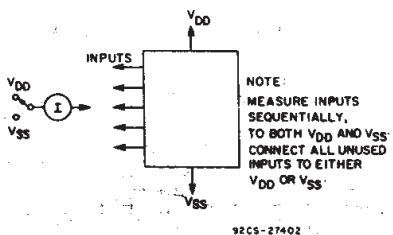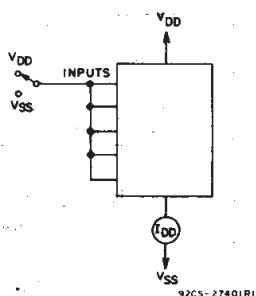
Fig. 15 — Quiescent device current test circuit.

92CS-27401RI

NOTE:
MEASURE INPUTS
SEQUENTIALLY,
TO BOTH V_{DD} AND V_{SS}.
CONNECT ALL UNUSED
INPUTS TO EITHER
V_{DD} OR V_{SS}.

92CS-27402

Fig. 16 — Input current test circuit.

NOTE:
TEST ANY COMBINATION
OF INPUTS

92CS-27441RI

Fig. 17 — Input-voltage test circuit.

TERMINAL ASSIGNMENTS

TOP VIEW

92CS-24536

CD4081B

TOP VIEW

NC=NO CONNECTION

92CS-24537R2

CD4082B

TOP VIEW

92CS-24538

CD4073B

Chip dimensions and pad layout
for CD4081B.

92CS-35100

Chip dimensions and pad layout
for CD4082B.

92CS-29275

Dimensions in parentheses are in
millimeters and are derived from
the basic inch dimensions as in-
dicated. Grid graduations are in
mils (10^{-3} inch).

Chip dimensions and pad layout
for CD4073B.

92CS-29276

3

COMMERCIAL CMOS
HIGH VOLTAGE ICs
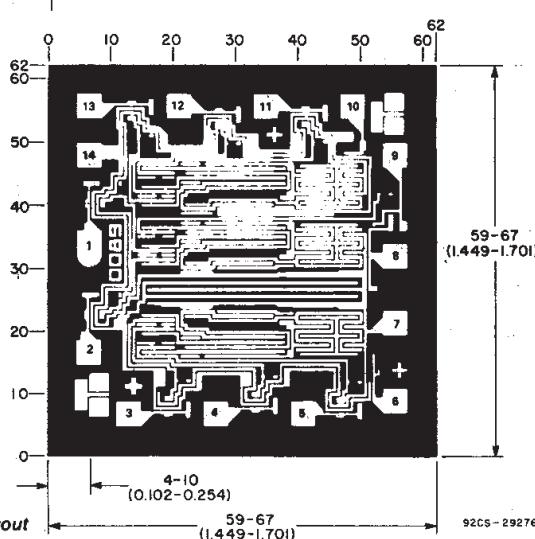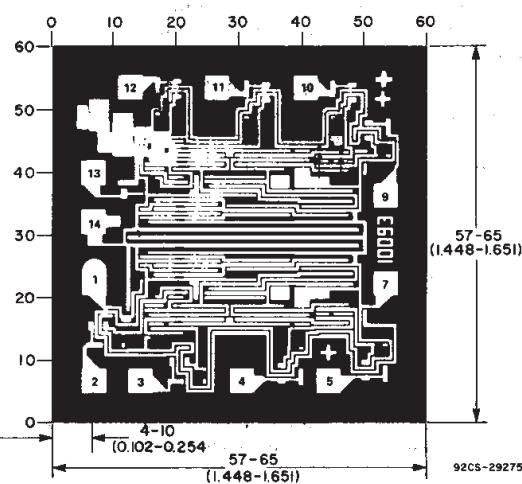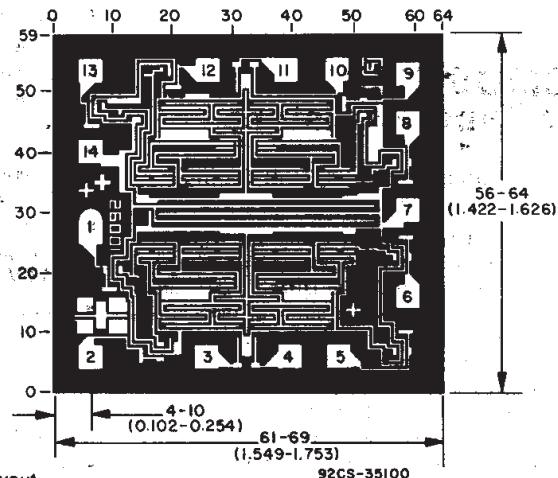
J (R−GDIP−T**)   CERAMIC DUAL IN−LINE PACKAGE
14 LEADS SHOWN
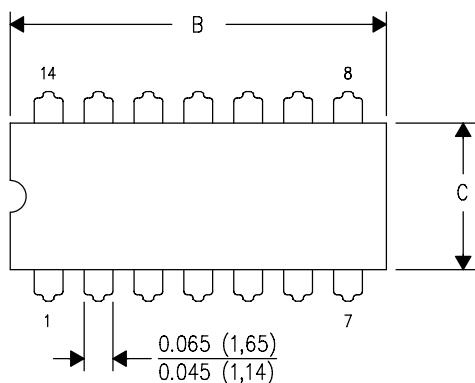
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

0.065 (1,65)
0.045 (1,14)

C

1   7

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

A

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

0°−15°

0.014 (0,36)
0.008 (0,20)
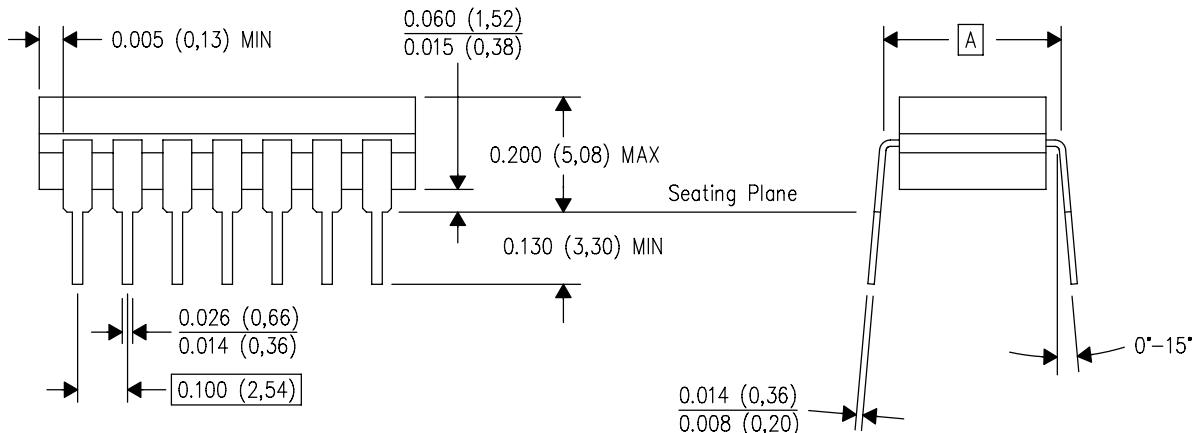
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. This package is hermetically sealed with a ceramic lid using glass frit.
          D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

MECHANICAL

MPDI002C – JANUARY 1995 – REVISED DECEMBER 20002

N (R-PDIP-T**)   PLASTIC DUAL-IN-LINE PACKAGE
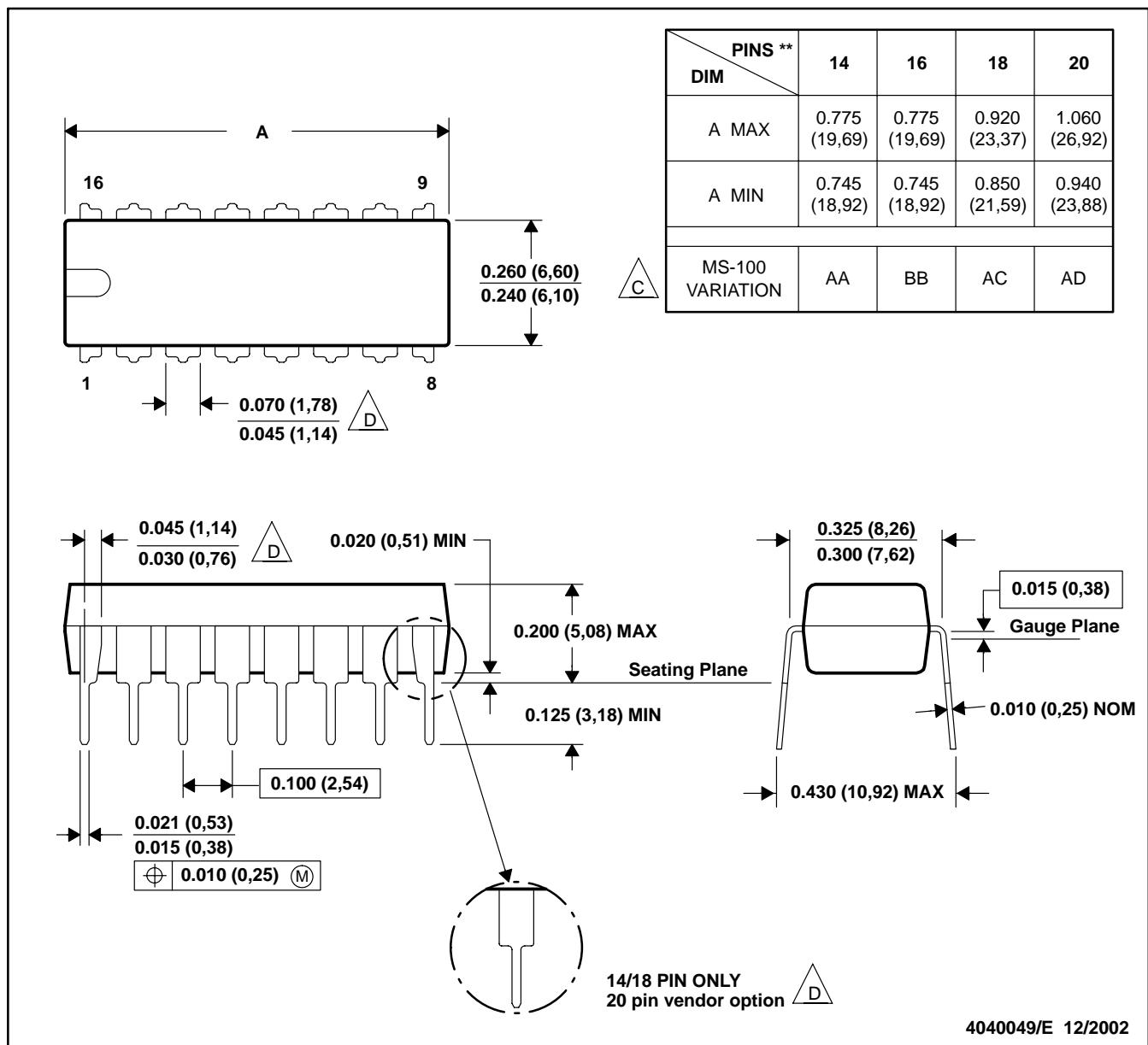
16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)
Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.430 (10,92) MAX

14/18 PIN ONLY
20 pin vendor option D

4040049/E 12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).
         D.   The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

1

MECHANICAL DATA

D (R-PDSO-G**) **PLASTIC SMALL-OUTLINE PACKAGE**

8 PINS SHOWN

0.050 (1,27)

0.020 (0,51) / 0.014 (0,35)

⊕ 0.010 (0,25)Ⓜ

8   5

0.244 (6,20) / 0.228 (5,80)

0.157 (4,00) / 0.150 (3,81)

1   4

A

0.008 (0,20) NOM

Gage Plane

0°– 8°

0.010 (0,25)

0.044 (1,12) / 0.016 (0,40)

0.069 (1,75) MAX

0.010 (0,25) / 0.004 (0,10)

Seating Plane

◠ 0.004 (0,10)

| PINS ** DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)
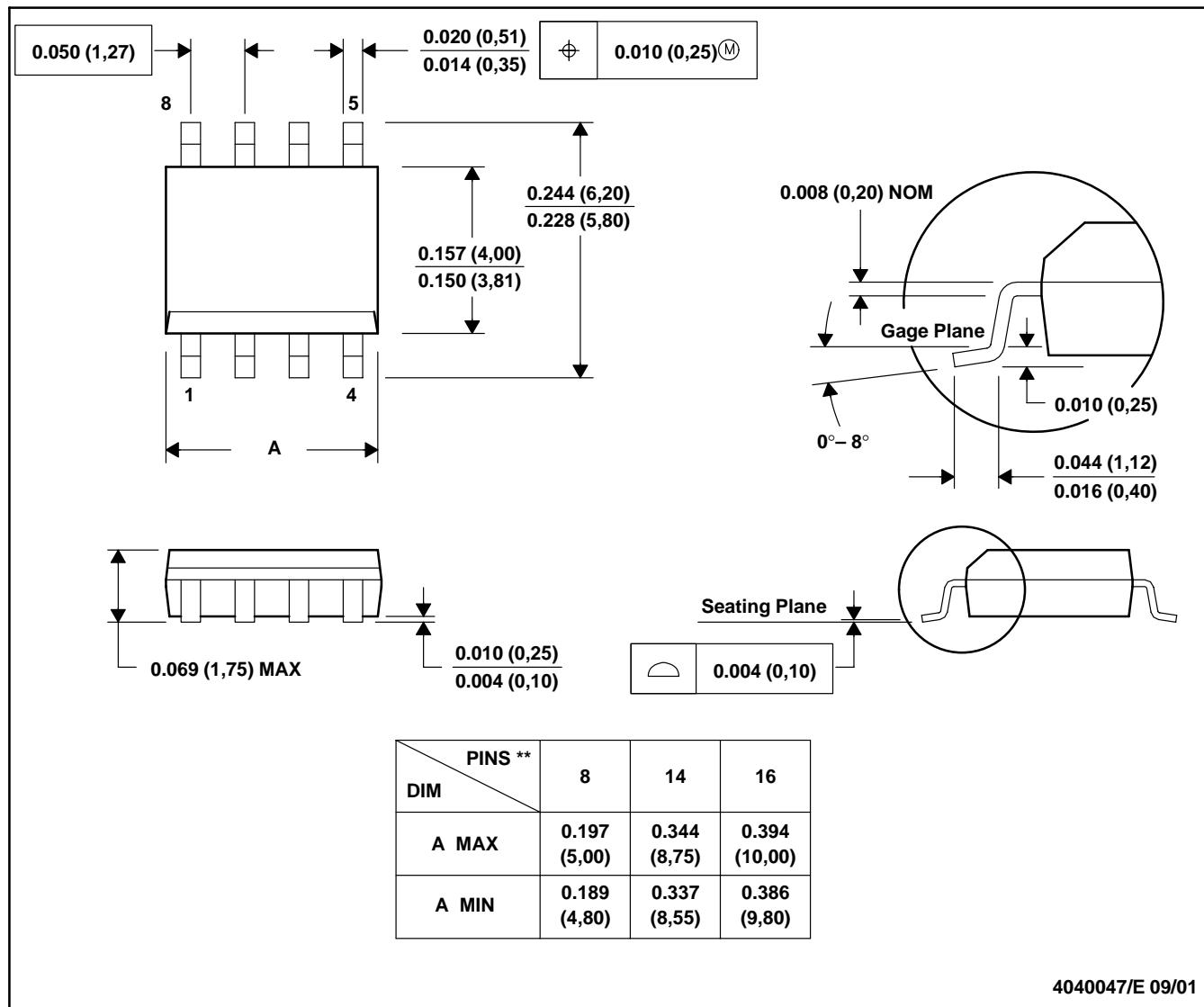
4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012
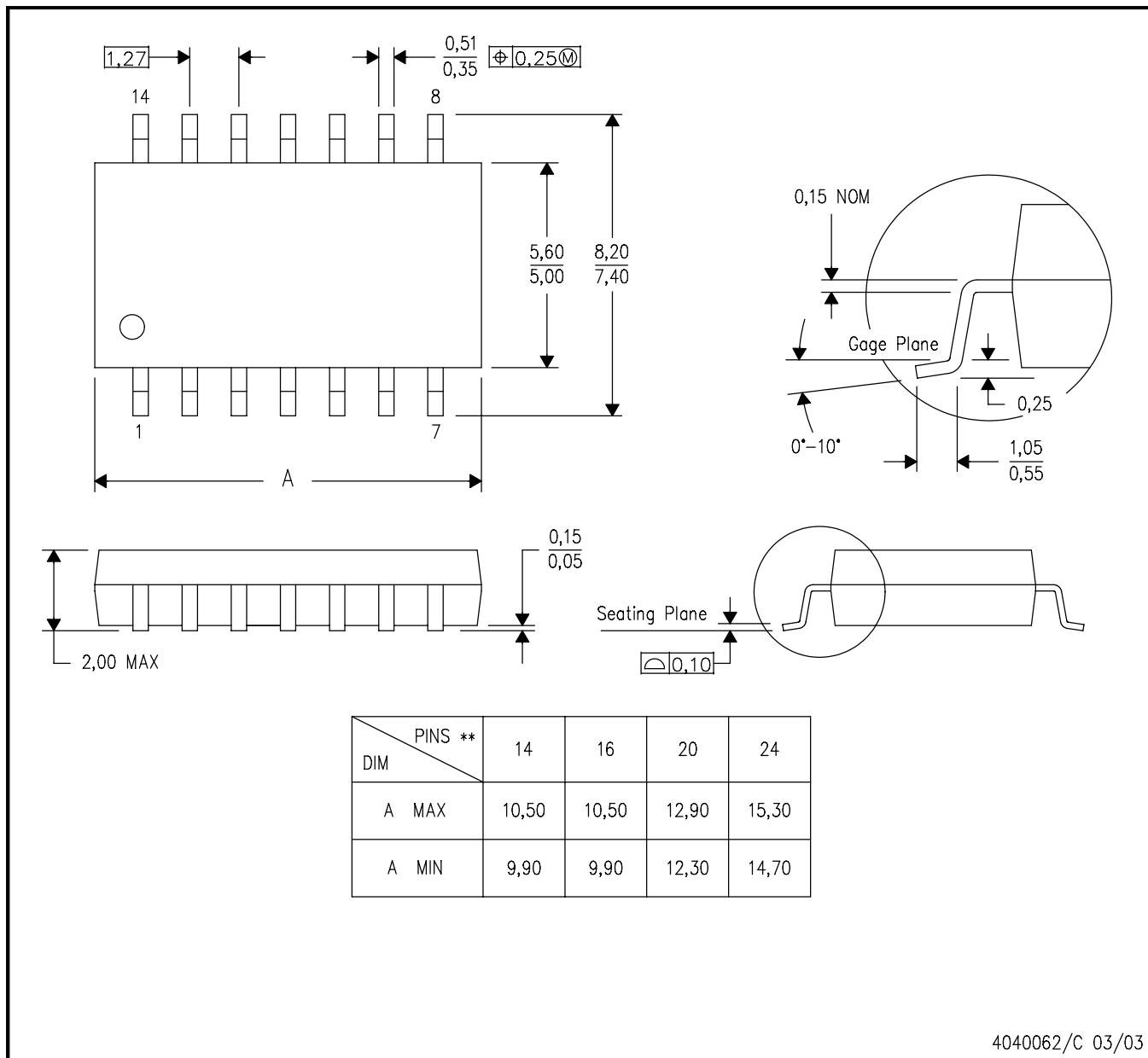
TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

1

NS (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

1,27

0,51
0,35

⊕ 0,25 Ⓜ

14   8

5,60   8,20
5,00   7,40

1   7

A

0,15 NOM

Gage Plane

0,25

0°–10°

1,05
0,55

0,15
0,05

2,00 MAX

Seating Plane

⬡ 0,10

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

PW (R-PDSO-G**) **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

1
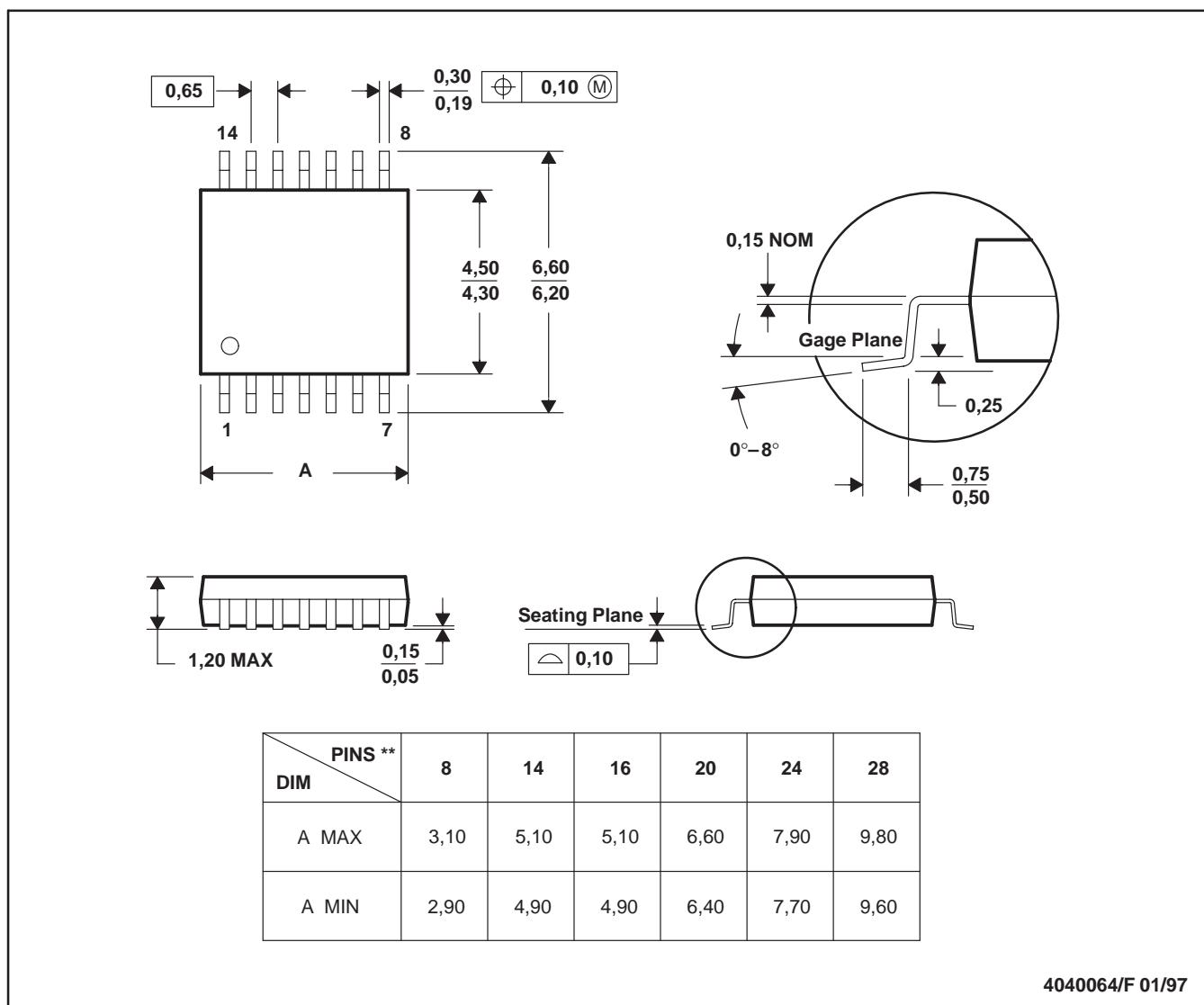
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